Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-68. (canceled)

69. (currently amended) A semiconductor chip with a wirebonded wire, ~~or wafer~~ comprising:

a silicon ~~semiconductor~~ substrate;

an active device ~~multiple transistors~~ in ~~or~~ and on said ~~semiconductor~~ silicon substrate;

a first dielectric layer over said silicon substrate;

an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region; ~~semiconductor substrate;~~

a second dielectric layer between said first and second metal layers;

a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region; ~~a contact point of said interconnecting metallization structure;~~

an aluminum cap ~~a first metal layer~~ comprising a first portion directly over said first region and a second portion directly over said passivation layer, wherein said aluminum cap is connected to said copper pad through said opening in said passivation layer, and wherein said aluminum cap has a width greater than that of said opening in said passivation layer; ~~contact point, wherein said first metal layer comprises aluminum; and~~

an adhesion/barrier layer on said aluminum cap; and

a gold layer on said adhesion/barrier layer and directly over said first and second portions of said aluminum cap, wherein said gold layer comprises an electroplated gold layer with a thickness between 2 and 20 micrometers, and wherein said wirebonded wire is joined with said gold layer.

~~a second metal layer over said first metal layer, wherein said second metal layer is used to be wirebonded thereto.~~

70. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip ~~or wafer~~.

71. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip ~~or wafer~~.

72. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said adhesion/barrier layer ~~interconnecting metallization structure~~ comprises tantalum. ~~copper.~~

73. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69~~, wherein said second metal layer comprises gold.~~ further comprising a polymer layer between said adhesion/barrier layer and said passivation layer, wherein said polymer layer has a thickness between 2 and 20 micrometers.

74. (currently amended) The semiconductor chip ~~or wafer~~ of claim 73, ~~69,~~ wherein said polymer layer comprises polyimide. ~~second metal layer comprises copper.~~

75. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69~~, wherein said second metal layer has a thickness of between about 2μm and 20μm.~~ further comprising a third dielectric layer on said gold layer, wherein an opening in said third dielectric layer is over said gold layer joined with said wirebonded wire.

76. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said gold layer joined with said wirebonded wire is directly over said active device. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises a titanium-tungsten alloy.~~

77. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said gold layer further comprises a gold seed layer under said electroplated gold layer. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises chromium.~~

78. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said adhesion/barrier layer ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer~~ comprises titanium.

79. (currently amended) The semiconductor chip ~~or wafer~~ of claim 69, wherein said active device comprises a transistor. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer has a thickness of between 2700 and 3300 Angstroms.~~

80. (currently amended) A semiconductor chip with a wirebonded wire, ~~or wafer~~ comprising:

a silicon ~~semiconductor~~ substrate;

an active device ~~multiple transistors~~ in ~~or~~ and on said silicon ~~semiconductor~~ substrate;

a first dielectric layer over said silicon substrate;

an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region; ~~semiconductor substrate;~~

a second dielectric layer between said first and second metal layers;

a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region; ~~a contact point of said interconnecting metallization structure;~~

an adhesion/barrier layer over said silicon substrate; and

a gold layer on said adhesion/barrier layer, wherein said gold layer comprises an electroplated gold layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer, and wherein said wirebonded wire is joined with said gold layer.

~~a first metal layer over said contact point, wherein said first metal layer comprises aluminum;~~

~~a second metal layer over said first metal layer; and~~

~~a wire wirebonded over said second metal layer.~~

81. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip ~~or wafer~~.

82. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip ~~or wafer~~.

83. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said adhesion/barrier layer ~~interconnecting metallization structure~~ comprises tantalum. ~~copper.~~

84. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80~~, wherein said second metal layer comprises gold.~~ further comprising a polymer layer between said adhesion/barrier

layer and said passivation layer, wherein said polymer layer has a thickness between 2 and 20 micrometers.

85. (currently amended) The semiconductor chip ~~or wafer~~ of claim 84, ~~80,~~ wherein said polymer layer comprises polyimide. ~~second metal layer comprises copper.~~

86. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80~~, wherein said second metal layer has a thickness of between about 2μm and 20μm.~~ further comprising a third dielectric layer on said gold layer, wherein an opening in said third dielectric layer is over said gold layer joined with said wirebonded wire.

87. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said gold layer joined with said wirebonded wire is directly over said active device. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises a titanium-tungsten alloy.~~

88. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said gold layer further comprises a gold seed layer under said electroplated gold layer, and wherein said electroplated gold layer has a thickness between 2 and 20 micrometers. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises chromium.~~

89. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said adhesion/barrier layer ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer~~ comprises titanium.

90. (currently amended) The semiconductor chip ~~or wafer~~ of claim 80, wherein said active device comprises a transistor. ~~further comprising a third metal layer between said first and second layers, wherein said third metal layer has a thickness of between 2700 and 3300 Angstroms.~~